AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An integrated circuit comprising:

a clock distribution network; and

an inductance control circuit coupled to the clock distribution network and receiving a clock signal, wherein the inductance control circuit, comprising an inductance, is configured to provide a resonant frequency of the clock distribution network as a function of a clock frequency of the clock signal [[.]] ; and

wherein the inductance of the inductance control circuit comprises:

an inductor coupled to the clock distribution network; and

a switchable bypass circuit coupled in parallel with the inductor.

2. (Original) The integrated circuit of claim 1, wherein the inductance provided by the inductance control circuit is adjustable.

3. (Original) The integrated circuit of Claim 1, wherein the inductance of the inductance control circuit is fixed.

4. (Original) The integrated circuit of Claim 1, wherein the integrated circuit is a programmable logic device.

5. (Cancelled)

6. (Original) The integrated circuit of Claim [[5]] 1, wherein the switchable bypass circuit is a pass gate.

7. (Original) The integrated circuit of Claim 6, wherein the first inductance control circuit further comprises a pass gate control circuit coupled to the pass gate.

8. (Original) The integrated circuit of Claim 7, wherein the pass gate control circuit is a configuration memory cell of an FPGA.

9. (Original) The integrated circuit of Claim 4, further comprising a second inductance control circuit coupled to the inductance control circuit.

10. (Original) The integrated circuit of Claim 9, further comprising a third inductance control circuit coupled to the second inductance control circuit, and wherein the third inductance control circuit is configurable to provide an inductance equal to a base inductance, the second inductance control circuit is configurable to provide an inductance equal to two times the base inductance, and the inductance control circuit is configurable to provide an inductance equal to four times the base inductance.

11. (Original) The integrated circuit of Claim 1, further comprising a capacitance control circuit coupled between the clock distribution network and ground.

12. (Original) The integrated circuit of Claim 11, wherein the capacitance control circuit comprises a capacitor coupled between the clock distribution network and ground.

13. (Original) The integrated circuit of Claim 12, wherein the capacitance control circuit further comprises a pass gate coupled between the capacitor and the clock distribution network.

14. (Original) The integrated circuit of Claim 13, wherein the capacitance control circuit further comprises a pass gate control circuit coupled to the pass gate.

15. (Original) The integrated circuit of Claim 14 wherein the pass gate control circuit is a configuration memory cell of an FPGA.

16. (Original) The integrated circuit of Claim 11 wherein the capacitance control circuit is adjustable.

17. (Original) The integrated circuit of Claim 1, wherein the function is an equivalence function.

18. (Currently Amended) A method to reduce power dissipation on a clock distribution network of an integrated circuit having a clock signal on the clock distribution network, the method comprising the steps of:

obtaining a clock frequency of the clock signal; and

varying an adjustable inductance coupled to the clock distribution network to substantially match a resonant frequency of the clock distribution network to the clock frequency[[.]] ; and

wherein the step of varying an adjustable inductance, comprises the steps of:

activating a first subset of controllable inductance circuits; and

deactivating a second subset of controllable inductance circuits.

19. (Original) The method of Claim 18, further comprising the step of calculating a network capacitance of the clock distribution network.

20. (Original) The method of Claim 18, further comprising the step of providing a capacitance on the clock distribution network.

21. (Cancelled)

22. (Currently Amended) An integrated circuit (IC) having programmable functions and programmable interconnections, comprising:

a clock distribution network coupled to a clock, the clock distribution network having an adjustable resonant frequency and the clock having a clock frequency; and

a tunable clock distribution system coupled between the clock and the clock distribution network, the tunable clock distribution system comprising a programmable inductance, wherein the programmable inductance is configured to change the adjustable resonant frequency to approach the clock frequency [[.]] ; and

wherein the tunable clock distribution system further comprises a programmable capacitance.

23. (Cancelled)

24. (Currently Amended) The IC of claim [[23]] 22, wherein the programmable capacitance is programmed using a configuration memory cell in the IC.

25. (Original) The IC of claim 22, wherein the programmable inductance is programmed using a configuration memory cell in the IC.

26. (New) An integrated circuit comprising:

a clock distribution network; and

an inductance control circuit coupled to the clock distribution network and receiving a clock signal, wherein the inductance control circuit, comprising an inductance, is configured to provide a resonant frequency of the clock distribution network as a function of a clock frequency of the clock signal; and

further comprising a capacitance control circuit coupled between the clock distribution network and ground; and

wherein the capacitance control circuit comprises a capacitor coupled between the clock distribution network and ground.